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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,176	04/06/2007	Ross Alan Kohler	Kohler 10-31-39	2823

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EXAMINER	
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ART UNIT	PAPER NUMBER
2827	

MAIL DATE	DELIVERY MODE
03/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/586,176	KOHLER ET AL.	
	Examiner	Art Unit	
	FERNANDO N. HIDALGO	2827	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 27 February 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-31*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

/AMIR ZARABIAN/
Supervisory Patent Examiner, Art Unit 2827

Continuation of 11. does NOT place the application in condition for allowance because: the remarks filed on 2/27/09, in regard to independent claims 1, 11, 21, 24 and 27, submit that the teachings of Reiner do not disclose "programming using hot carrier." As well known in the art, and incidentally finding support in paragraph [0018] of the specifications of the instant application, hot carrier effects, normally caused over time in the routine use of a transistor, can be accelerated by the use of high voltage biasing thus causing channel degradation at a drain/source junction by the voltage biasing thereto. Page 4 of Reiner, furthermore, exemplarily teaches that high voltage levels result in degradation of the memory device due to an increased heating of the carrier (hot carrier effecs) in agreement, but anticipating the teachings found in paragraph [0018] of the instant application. Reiner further teaches on page 4: "Hot carrier effects occur ... It has thus to be ensured that no inolerable degradation of the memory circuit occurs .." That is, unquestionably and objectively clear that hot carrier effects occur and that intolerable degradation (memory rendered useless in plain language) occurance is to be avoided. Therefore, contrary to the submission in the remarks that Reiner teaches away "by teaching to avoid hot carrier conditions," Reiner, in fact, teaches programming, wherein hot carrier effects occur, but sensibly cautions that no INTOLERABLE DEGRADATION be permitted, degradation that would render the memory device useless, inoperable. The remarks further suggest that there was no reason to combine the prior art references used because there is no suggestion in Reiner of using hot carrier techniques. This conclusion is irrational in view of the clearly estabished teachings of hot carrier effects in OTP memory as taught at least by Reiner. Page 10 of the remarks submit that Reiner does not overcome the claim of a memory cell, comprising only one transistor of claim 24. Reiner, at least on page 5, teaches "a memory transistor T2." A select transistor, for selectively programming the one memory transistor, is available. This is no different from the instant application, wherein in at least the Abstract and paragraph [0006] it is disclosed that "transistors in the array are selectively programmed: "The present invention recognizes that such characteristics changes can be SELECTIVELY applied to memory cells in the OTP memory devices ..." That is both the OTP of Reiner and the OTP of the instant application have a one transistor memory selectively programmed by inherent means such as a select transistor. Inherently, there is absolutelly no way, technique, manner or method that would progam a one-transistor memory without means for first selecting it for applying voltage biasing conditions. In regard to the rejection of claim 27, the remarks submit, incomprehensibly, that the preamble of said claim, "An integrated circuit," is not taught by the prior art references. Reiner, in at least page 2, lines 4-8, and page 6, lines 20-21, teaches what is inherent in semiconductor circuit design in general and OTP memory in particular: programming means for applying voltages to the OTP memory and readout means (sense amplifier circuitry) for reading the OTP memory. Unquestionably, these means and the OTP memory are inherent parts of an integrated circuit. Any claims to the contrary are suspect at best. In regard to at least dependent claims 3, 13, 23 and 29, the remarks submit that Reiner does not teach "said altered characteristics." On the contrary, Reiner is amply clear, on page 7, that programmability of the memory cell can be determined by the anount of current passing through the memory channel: below a predetermined detection level is considered no programming, above said level is considered programming. Furthermore, it is well known in the art, unquestionably to one of ordinary skill in said art, that threhold voltage is in direct relationship to the current through a transistor channel. This is inherently so whether the transistor is in normal use (no prevalent hot carrier effects) or when bot carrier effects are involved. In regard to dependent claims 4 and 14, the remarks submit that Reiner does not teach programming applting a stressful voltage to a drain and a gate. Reiner, contrary to this assertion, teaches in at least page 4 a high drain voltage and a moderate gate voltage in order to induce hot carrier effects, as such the drain and gate voltages are stressful enough. In reagard to dependent claims 5, 15 and 30, Reiner in at least page 6 teaches "A subsequent readout of the memory by readout means (sensing detection) of the current (thus threshold) of the memory. In regard to dependent claims 7, 17 ,31, 8 ,18, 9 and 19, it is believed sufficient analysis of the teachings of Reiner has been presented as set forth above. In regard to dependent claims 10 and 20, the remarks submit that Reiner does not teach or mention rows or raising the gate terminal. In any memory array, memory elements of cells are inherently organized in rows and columns. FIG. 5A is one example of a memory cell addressed by rows and columns and Reiner in at least page 2 teaches applying a gate voltage on the memory cell. These teachings contradict the submission on page 13 of the remarks. Finally, as set forth above, it is believed the instatn application, as claimed, is in no better condition for allowance. .